



FORM PTO-1449/A and B (Mod 10/99) INFORMATION DISCLOSURE STATEMENT BY APPLICANT		APPLICATION NO.: 09/842,312		ATTY. DOCKET NO.: S1022.80655US00	
		FILING DATE: April 25, 2001		CONFIRMATION NO.: 6679	
		APPLICANT: Andrew C. STURGES			
		GROUP ART UNIT: 2183		EXAMINER: Richard L. Ellis	
Sheet	1	of	1		

U.S. PATENT DOCUMENTS

Examiner's Initials	Cite No.	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication or of issue of Cited Document MM-DD-YYYY
		Number	Kind Code		
RLE	A1*	3,426,330	—	H.B. Marx, et al.	01-02-1969
RLE	A2*	3,573,854	—	Watson, et al.	04-06-1971
RLE	A3*	4,974,155	—	Dulong, et al.	11-27-1990
RLE	A4*	5,615,386	—	Amerson, et al.	03-25-1997
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FOREIGN PATENT DOCUMENTS

Examiner's Initials	Cite No.	Foreign Patent Document			Name of Patentee or Applicant of Cited Document (not necessary)	Date of Publication of Cited Document MM-DD-YYYY	Translation (Y/N)
		Office/ Country	Number	Kind Code			
RLE	B1*	EP	A-0 355 069	—	Evans & Sutherland Computer Corp.	02-21-1990	—
RLE	B2*	EP	A-0 219 203	—	Case et al.	02-15-1995	—
✓							—

OTHER ART — NON PATENT LITERATURE DOCUMENTS

Examiner's Initials	Cite No	Include name of the author (in CAPITAL LETTERS) title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, relevant page(s), volume-issue number(s), publisher, city and/or country where published.	Translation (Y/N)
RLE	C1*	European Search Report from United Kingdom Patent Application Number 9412487.2, filed June 22, 1994.	—
RLE	C2*	International Journal Of Mini And Microcomputers, vol. 11, no. 1, 1989, Calgary, California US, pp 13-17. Cortadella and Llaberia "Making Branches Transparent To the Execution Unit".	—
RLE	C3*	Proceedings 4th MIT Conference: Advanced Research In VLSI, April 7, 1986, Cambridge, MA, US pp 73-88, Plaszkun and Farrens "An Instruction Cache Designs For Use With a Delayed Branch".	—
RLE	C4*	IBM Technical Disclosure Bulletin, vol. 14, no. 12, May 1972, New York, US, pp 3599-3611, Beebe et al, "Instruction Sequencing Control".	—
RLE	C5*	Computer Architecture: A Quantitative Approach, David A. Patterson, et al., pages 265-270 (Chapter 6, Sectopm 4); no date provided	—
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EXAMINER: <u>Richard Ellis</u>	DATE CONSIDERED: <u>8/25/2004</u>	Technology Center 2100
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#EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

*a copy of this reference is not provided as it was previously cited by or submitted to the office in a prior application, Serial No. 09/356,122, filed July 16, 1999, and relied upon for an earlier filing date under 35 U.S.C. 120 (continuation, continuation-in-part, and divisional applications).

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